ABSTRACT OF THE DISCLOSURE

Methods and apparatus are described to facilitate forming memory devices with low resistance polysilicon local interconnects that allow a smaller array feature size and therefore facilitate forming arrays of a denser array format. Embodiments of the present invention are formed utilizing a wet etch process that has a high selectivity, allowing the deposition and etching of polysilicon local interconnects to source regions of array transistors. By providing for a local interconnect of polysilicon, a smaller source region and/or drain region can also be utilized, further decreasing the required word line spacing. Low resistance polysilicon local source interconnects can also couple to an increased number of memory cells, thereby reducing the number of contacts made to an array ground.